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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,563	01/30/2004	Cesare Ronsisvalle	856063.761	5861
38106	7590	09/09/2005		
SEED INTELLECTUAL PROPERTY LAW GROUP PLLC 701 FIFTH AVENUE, SUITE 6300 SEATTLE, WA 98104-7092				
			EXAMINER	
			DICKEY, THOMAS L	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



## Office Action Summary

Application No.

10/769,563

Applicant(s)

RON SISVALLE, CESARE

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2005.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-9 and 12-16 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) 7, 8 and 13-16 is/are allowed.  
6) ☐ Claim(s) 1-3, 5, 6, 9 and 12 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

*Minhloan Tran*  
**Minhloan Tran**  
**Primary Examiner**  
**Art Unit 2826**

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 30 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

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## DETAILED ACTION

1. The amendment filed on 06/29/05 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

- A.** Claims 1,2,5, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Luoni et al. (5,883,537).

Luoni et al. discloses an emitter switching configuration, comprising at least one bipolar transistor Q and a MOS transistor T<sub>m</sub> having a common conduction terminal D; and a Zener diode nZ inserted between a control terminal (no part # in the figure – it is seen as the node between the base of the transistor Q and the anode of Zener diode nZ) of said bipolar transistor Q and said common conduction terminal D, said Zener diode nZ having an anode terminal (note that the anode and cathode are clearly marked in the figure, using standard symbols) connected to said control terminal (no part # in the figure) of said bipolar transistor Q and a cathode terminal connected to said common conduction terminal D of said bipolar transistor Q, wherein said Zener diode nZ has a lower

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Zener voltage than a breakdown voltage of a junction between said control terminal (no part # in the figure) and said common conduction terminal D of said bipolar transistor Q, said MOS transistor T<sub>m</sub> has a low breakdown voltage, and said MOS transistor T<sub>m</sub> is of the vertical double-diffusion type. Note figure 2 and column 3 lines 29-60 of Luoni et al.

**B.** Claims 1,3,9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Majumdar (4,777,386).

With regard to claims 1 and 3 Majumdar discloses an emitter switching configuration, comprising at least one bipolar transistor Q1 and a MOS transistor (part of base drive circuit 1– note that the MOS transistor is connected to bipolar transistor Q1 at B2, the base, and at E2, the emitter) having a common conduction terminal E2; and a Zener diode 15 inserted between a control terminal B2 of said bipolar transistor Q1 and said common conduction terminal E2, said Zener diode 15 having an anode terminal (note the figure to see which end is the anode and which is the cathode – the diode is clearly marked) connected to said control terminal B2 of said bipolar transistor Q1 and a cathode terminal (note the figure) connected to said common conduction terminal E2 of said bipolar transistor Q1, wherein said common conduction terminal E2 corresponds to an emitter terminal of said bipolar transistor Q1 and to a drain terminal of said MOS transistor (part of base drive circuit 1). Note figure 1 and column 3 lines 6-47 of Majumdar.

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With regard to claims 9 and 12 Majumdar discloses an emitter switching circuit, comprising a bipolar transistor Q1 having a base-to-emitter device 15-16 coupled to a drain terminal of a MOS transistor (part of base drive circuit 1 – note that the MOS transistor is connected to bipolar transistor Q1 at B2, the base, and at E2, the emitter) and configured to prevent a breakdown condition of a body-drain junction of the MOS transistor (part of base drive circuit 1), the base-to-emitter device 15-16 comprising a Zener diode 15 having an anode terminal connected to a base terminal of the bipolar transistor Q1 and a cathode terminal connected to an emitter terminal of the bipolar transistor Q1. Note figure 1 and column 3 lines 6-47 of Majumdar.

***Allowable Subject Matter***

3. Claims 7,8, and 13-16 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an emitter switching configuration, comprising at least one substrate in which are formed second wells of first conductivity type, adjacent to first wells of second conductivity type and in contact with said first wells and with a second buried layer to define a Zener diode parallel to a junction defined by a first buried layer and said second buried layer with an anode of the Zener diode coupled to a control terminal of a bipolar transistor and a cathode coupled to a common conduction terminal where the emitter of the bipolar transistor is connected to the drain of a MOSFET, as recited in claims 7 and 13.

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***Response to Arguments***

4. Applicant's arguments with respect to claims 1-3,5,6,9, and 12 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is

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571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**TLD**  
**08/05**